What is claimed is:

- 1 1. A digital image processing device comprising:
- 2 a signal processing unit to process a video input signal;
- a frame memory to store a result from the processing
- 4 performed by said signal processing unit; and
- a redundant pixel embedding circuit to embed a redundant
- 6 pixel not to be displayed in an image line read from said frame
- 7 memory and to produce a video output signal.
- 1 2. The digital image processing device according to Claim 1,
- 2 wherein said redundant pixel embedding circuit has a function of
- 3 receiving, as an input, an image line read from said frame memory
- 4 and of embedding, according to an embedding control signal fed
- 5 from outside, a redundant pixel in a specified position in said
- 6 image line.
- 1 3. A digital image processing device comprising:
- 2 a signal processing unit to process a video input signal;
- a frame memory to store a result from the processing
- 4 performed by said signal processing unit;
- 5 a serial-parallel converting circuit to receive image data
- 6 read from said frame memory in a time-series manner and to produce
- 7 an output making up an image line,
- a redundant pixel embedding circuit to embed a redundant
- 9 pixel not to be displayed in said image line and to output data,
- 10 and
- 11 a parallel-serial converting circuit to output said image

- 12 line in which said redundant pixel is embedded as time-series
- 13 image data.
 - 1 4. The digital image processing device according to Claim 3,
 - 2 wherein said serial-parallel converting circuit which is made up
 - 3 of a register file being able to store an image line and which
 - 4 has a function of sequentially storing image data fed from said
 - 5 frame memory in a time-series manner according to a writing
 - 6 control signal fed from outside and of reading, simultaneously
 - 7 and in parallel, contents of all registers in said register file.
 - 1 5. The digital image processing device according to Claim 3,
 - 2 wherein said redundant pixel embedding circuit has a function of
 - 3 receiving, as an input, said image line read from said
 - 4 serial-parallel converting circuit and of embedding, according
 - 5 to an embedding control signal fed from outside, a redundant pixel
 - 6 in a specified position in said image line.
 - 1 6. The digital image processing device according to Claim 3,
 - 2 wherein said parallel-serial converting circuit has a register
 - 3 file made up of two or more shift registers and a selector to select
 - 4 an output from each of said shift registers and to output the
 - 5 selected output and wherein said register file is able to store
 - 6 an image line in one clock cycle and wherein each of said shift
 - 7 registers is able to perform a shifting operation, according to
 - 8 a reading control signal fed from outside, in synchronization with
 - 9 a clock signal and wherein said selector has a function of
- 10 selecting a specified shift output from said shift register and
- 11 of outputting the selected output according to an embedding

- 12 control signal fed from outside.
 - 1 7. The digital image processing device according to Claim 6,
 - 2 wherein each of said shift registers is made up of two or more
 - 3 split shift registers and wherein each of said split shift
 - 4 registers receives a data input, shift data input, latch signal
 - 5 input, and shift signal input and produces a shift data output
 - 6 and wherein each of said shift registers has a function of writing,
 - 7 when data is to be written to said split shift registers, data
 - 8 at one time, by making active a latch signal input, in
 - 9 synchronization with a clock and, at time of shifting operations,
- 10 of performing said shifting operation for data, by making active
- 11 a shift signal input, in synchronization with a clock and of
- 12 feeding a shift output fed from each of said split shift registers
- 13 to said selector by connecting a terminal for a shift output from
- 14 each of said split shift registers to a terminal for a shift input
- 15 of each of adjacent split shift registers to allow said shift
- 16 register to perform said shift operation as a whole.
 - 1 8. A digital image processing device comprising:
 - 2 a signal processing means to process a video input signal;
 - a frame memory to store a result from the processing
 - 4 performed by said signal processing means; and
 - 5 a redundant pixel embedding means to embed a redundant pixel
 - 6 not to be displayed in an image line read from said frame memory
 - 7 and to produce a video output signal.
 - 1 9. The digital image processing device according to Claim 8,
 - 2 wherein said redundant pixel embedding means has a function of

- 3 receiving, as an input, an image line read from said frame memory
- 4 and of embedding, according to an embedding control signal fed
- 5 from outside, a redundant pixel in a specified position in said
- 6 image line.
- 1 10. A digital image processing device comprising:
- 2 a signal processing means to process a video input signal;
- a frame memory to store a result from the processing
- 4 performed by said signal processing means;
- a serial-parallel converting means to receive image data
- 6 read from said frame memory in a time-series manner and to produce
- 7 an output making up an image line,
- a redundant pixel embedding means to embed a redundant pixel
- 9 not to be displayed in said image line and to output data, and
- 10 a parallel-serial converting means to output said image
- 11 line in which said redundant pixel is embedded as time-series
- 12 image data.
- 1 11. The digital image processing device according to Claim 10,
- 2 wherein said serial-parallel converting means which is made up
- 3 of a register file being able to store an image line and which
- 4 has a function of sequentially storing image data fed from said
- 5 frame memory in a time-series manner according to a writing
- 6 control signal fed from outside and of reading, simultaneously
- 7 and in parallel, contents of all registers in said register file.
- 1 12. The digital image processing device according to Claim 10,
- 2 wherein said redundant pixel embedding means has a function of
- 3 receiving, as an input, an image line read from said serial-

- 4 parallel converting means and of embedding, according to an
- 5 embedding control signal fed from outside, a redundant pixel in
- 6 a specified position in said image line.
- 1 13. The digital image processing device according to Claim 10,
- 2 wherein said parallel-serial converting means has a register file
- 3 made up of two or more shift registers and a selector to select
- 4 an output from each of said shift registers and to output the
- 5 selected output and wherein said register file is able to store
- 6 an image line in one clock cycle and wherein each of said shift
- 7 registers is able to perform a shifting operation, according to
- 8 a reading control signal fed from outside, in synchronization with
- 9 a clock signal and wherein said selector has a function of
- 10 selecting a specified shift output from said shift register and
- 11 of outputting the selected output according to an embedding
- 12 control signal fed from outside.
 - 1 14. The digital image processing device according to Claim 13,
 - 2 wherein each of said shift registers is made up of two or more
 - 3 split shift registers and wherein each of said split shift
 - 4 registers receives a data input, shift data input, latch signal
 - 5 input, and shift signal input and produces a shift data output
 - 6 and wherein each of said shift registers has a function of writing,
 - 7 when data is to be written to said split shift registers, data
 - 8 at one time, by making active a latch signal input, in
 - 9 synchronization with a clock and, at time of shifting operations,
- 10 of performing said shifting operation for data, by making active
- 11 a shift signal input, in synchronization with a clock and of
- 12 feeding a shift output fed from each of said split shift registers

- 13 to said selector by connecting a terminal for a shift output from
- 14 each of said split shift registers to a terminal for a shift input
- 15 of each of adjacent split shift registers to allow said shift
- 16 register to perform said shift operation as a whole.